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# Challenge to the Barrier of Conduction Loss in PiN Diode toward $V_F < 300$ mV with Pulsed Carrier Injection Concept

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**Abstract**—Threshold voltage of 0.8 V in forward current conduction in PiN diodes has become a major problem in the efficiency improvement in power electronics systems. This paper challenges to minimize the conduction loss in PiN diode by employing newly proposed pulsed carrier injection mechanism, targeting effective forward voltage drop about a half of the PiN diode threshold voltage of 0.8 V. Under TCAD basis simulation, the authors successfully demonstrated the concept obtaining conduction voltage drop as low as 270 mV at 50 A/cm<sup>2</sup> for 930 V blocking voltage devices.

## I. INTRODUCTION

The large losses with PiN diodes are one of the bottle necks in the efficiency improvement in power electronics systems. Specially, the losses with the threshold voltage of 0.8 V in forward conduction share major part of power semiconductor losses. Theoretically, the threshold voltage appears in current conduction across the PiN structure [1] [2] and the voltage has been recognized as the “Silicon limit” in bipolar devices such as PiN diodes, IGBTs and thyristors.

The authors propose a new diode concept to reduce the diode conduction losses (Fig. 1). The proposed diode operates in transient way under forward conduction. The diode has a special structure in the anode side to inject holes in pulse wise during forward conduction, while conventional PiN diode injects holes steady state way. In between the hole injection-pulse, electron current is bypassed through the extra N-layer in the anode side. Since the conduction threshold voltage of 0.8 V appears during the hole-injection pulse and the threshold voltage vanishes when the electron current bypassed through the N-layer so that the average forward voltage drop can be reduced below 0.8 V.

This paper is organized as follows. Firstly the pulsed carrier injection concept and the mechanism of reducing the average forward voltage drop are explained. Secondly the method and results of TCAD basis simulation to confirm the feasibility of the pulsed carrier injection concept are shown. Finally the authors describe the optimum condition of the

frequency and the width of the pulse. The results of this simulation are shown.

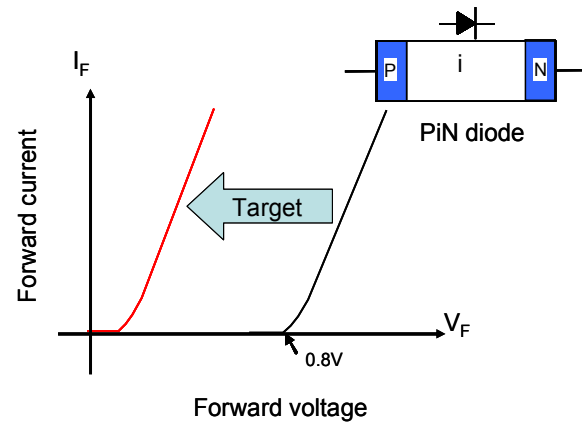


Figure 1. The structure and forward characteristic of conventional PiN diode and the target of this study. Conduction threshold voltage of about 0.8 V appears in PiN diode with current flowing across the PN junction.

## II. PULSED CARRIER INJECTION CONCEPT

In the forward conduction of the proposed device, holes are injected into the i-layer in pulse wise with MHz range frequency, which is the major difference from conventional PiN diodes in which forward conduction the holes are injected steadily during forward bias condition. In the new concept device, the PiN diode structure and NiN structure are integrated, so that the device operates PiN diode mode for carrier injection to storage in the i-layer and NiN-mode for newly introduced conduction mode, alternately. The NiN-mode is introduced to cancel the PiN diode threshold voltage of 0.8 V by removing the PN junction in the forward current path.

Figure 2 schematically illustrates a device structure example and explains the operation mechanism. The device has a PiN diode structure with N<sup>+</sup> - layer next to the P-emitter

to bypass the electron current from the i-layer to the anode side. In the PiN-mode, holes are injected in the i-layer and the stored carrier in the anode side of the i-layer increases with time. In the NiN-mode, on the other hand, hole injection is stopped and electron in the i-layer is bypassed to the extra  $N^+$ -layer located next to the P-emitter. Since, no holes are injected, the stored carrier gradually reduced with time in the anode side of the i-layer. In this mode, only electrons contribute the conduction at the both side of the i-layer and thus no PN junction operation appears along the current path. Therefore, it is expected that the threshold voltage of 0.8 V will not be appeared during this mode. During the forward current conduction, the device operates in the PiN-mode and the NiN-mode alternately in high frequency by external switches. The average forward voltage drop will decrease thanks to the NiN-mode operation.

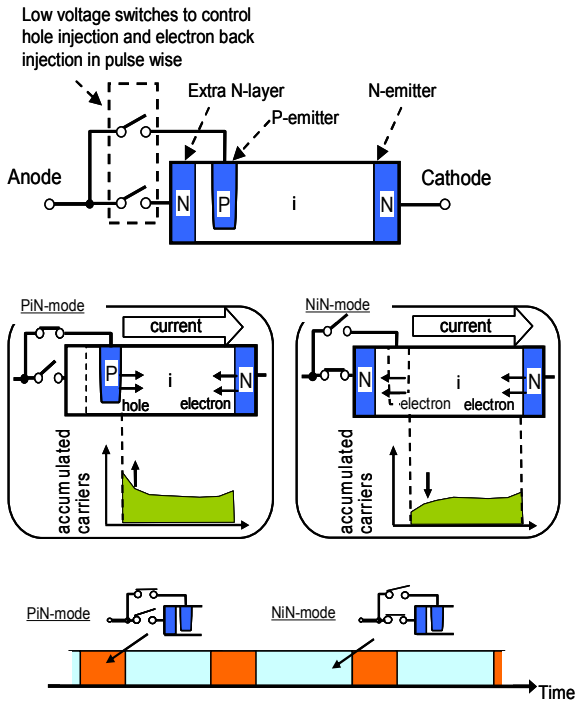


Figure 2. The concept of forward voltage drop reduction. Holes are injected pulse-wise. During PiN-mode holes are injected and alternatively only electrons flow during NiN-mode. Since no PN junction exists along the current flow, no conduction threshold voltage appeared. The two switches in anode side require low blocking voltage of about 2 V.

The required voltage range of the external switch can be below 10 V because the switches are connected to the high voltage diode in series.

### III. SIMULATION

The concept is demonstrated numerically with a TCAD simulator [3]. In the simulation, the impurity concentration and length of the i-layer are  $1 \times 10^{16} \text{ cm}^{-3}$  and 56  $\mu\text{m}$ . The simulated blocking voltage was 930 V under unconnected condition for the extra N-layer as shown in Fig. 3.

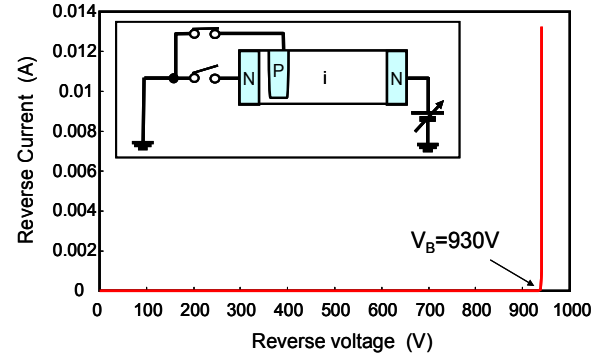


Figure 3. TCAD simulation result of blocking voltage. At the reverse bias, proposed diode is fixed PiN-mode.

Figure 4 shows the simulation result of transient forward voltage drop of proposed diode for condition under hole injection pulse (PiN-mode) interval of 25 ns and 125 ns for the NiN-mode. The current density is  $50 \text{ A/cm}^2$ . Forward voltage drop is about 0.8 V during the PiN-mode. The voltage drop in the NiN-mode is dramatically reduced to about 0.2 V comparing to PiN diodes. Since the PiN-mode conduction time is chosen much shorter than the NiN-mode, the average forward voltage drop is as low as 270 mV for this case. Ideal switches are used in the simulation for the external low voltage switches for alternating the PiN-mode and the NiN-mode.

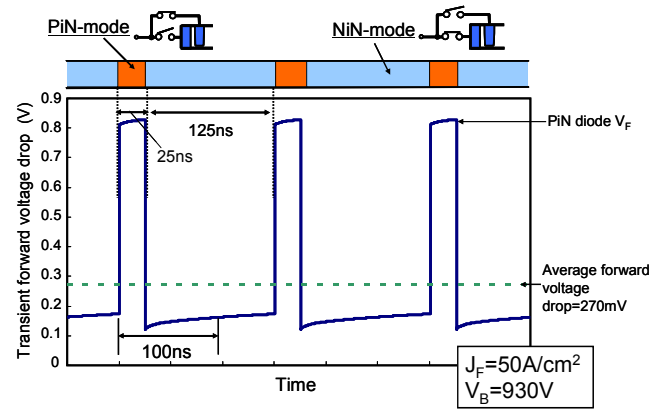


Figure 4. TCAD simulation result of transient forward voltage drop of proposed diode (the diode has  $V_B=930 \text{ V}$ ). The forward voltage is below 200 mV during NiN-mode since no PN junction appears along the current path, while the 0.8 V voltage drop appears during PiN-mode. The average value of forward voltage drop is as low as 270 mV.

Figure 5 shows the behavior of stored carrier in the anode side of the i-layer. The stored carrier increases with time during the PiN-mode with the hole injection from the P-emitter (see curves a and b in the figure). The stored carrier turns to decrease during the NiN-mode due to the lack of hole injection from the P-emitter (see curves c, d, e and f in the figure). With the cycle wise operation of the PiN-mode and

the NiN-mode maintains sufficient level of carrier storage in the i-layer for low the conduction resistance in the i-layer.

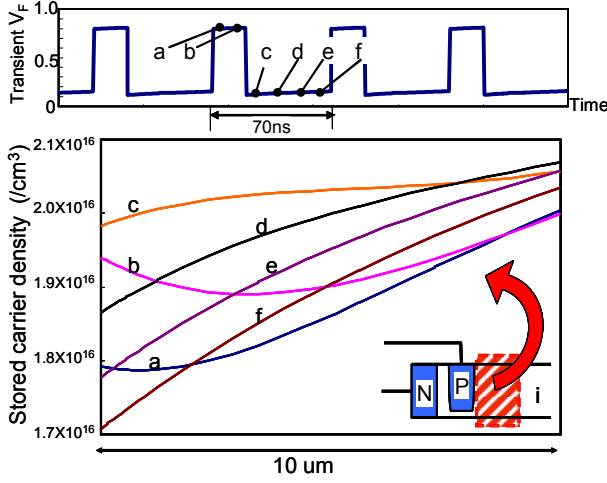


Figure 5. Transient stored carrier distribution during one cycle of PiN-mode and NiN-mode. Carrier density increases during PiN mode and decreases during NiN mode. It should be noted that the sufficient amount of carrier is stored through out the time of the cycle (TCAD simulation).

Optimum pulse pattern is investigated. Figure 6 shows the simulated average forward voltage as functions of the ratio of PiN-mode time in one cycle of time for the PiN-mode and the NiN-mode. Since the voltage drop during the NiN-mode shows about 0.2 V and 0.8 V for the PiN-mode, decrease of the PiN-mode ratio reduces the average forward voltage drop. Further decrease of PiN-mode result in the increase of the voltage due to the decrease of the stored carrier inside the i-layer with too small amount of hole injection to maintain low resistance current conduction in the i-layer.

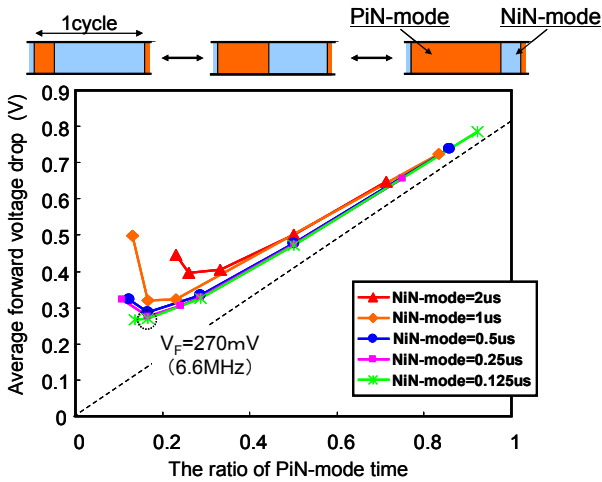


Figure 6. TCAD simulation results of average forward voltage drop for the diode with the pulsed carrier injection as a function of PiN-mode time in the cycle. Frequencies of the pulse cycle are also described in the figure. Increasing the pulse frequency, the optimum average forward voltage drop decreases

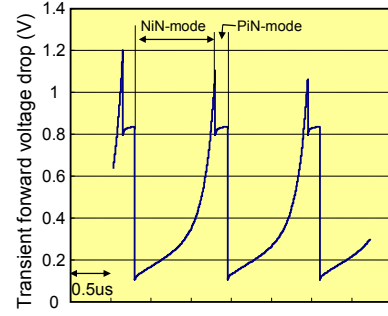


Figure 7. Transient forward voltage drop for a short PiN-mode condition. Because of smaller amount of hole injection, transient voltage increases with time during NiN mode.

Figure 7 shows the waveform for a short PiN-mode condition. The transient forward voltage drop increases with time during the NiN-mode due to the decrease of stored carrier in the i-layer.

A remarkable low average forward voltage drop of 270 mV is obtained under the condition of 25 ns for the PiN-mode and 125 ns for the NiN-mode for conduction current density of 50 A/cm<sup>2</sup>. Increasing the pulse frequency, the optimum average forward voltage significantly improved.

Figure 8 shows forward V-I characteristics of the proposed diode comparing with that of conventional PiN diode. The average forward voltage drop for the proposed diode is lower than half of the conventional PiN diode even in high current region of 80 A/cm<sup>2</sup>.

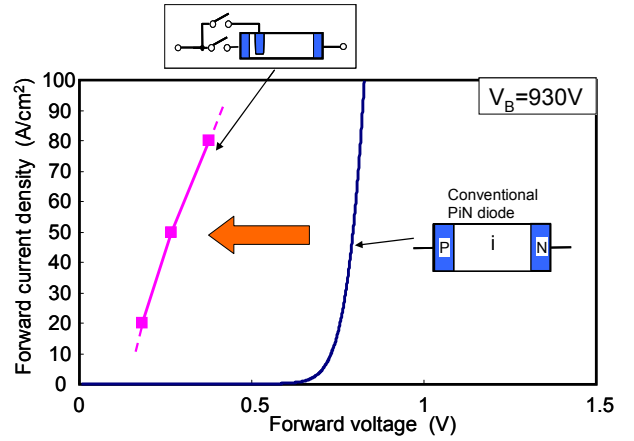


Figure 8. The forward characteristic of proposed concept diode for, PiN-mode time:25 ns and NiN-mode time:125 ns obtained by TCAD simulation.

#### IV. CONCLUSIONS

The authors propose a new diode concept to reduce the diode conduction losses. In the new concept device, the PiN diode structure and NiN structure are integrated so that the device operates PiN diode mode for carrier injection and NiN-mode to cancel the threshold voltage of 0.8 V by removing the PN junction in the forward current path.

The concept is confirmed by the simulation and a remarkable low average forward voltage drop of 270 mV is obtained under the condition of 25 ns for the PiN-mode and 125 ns for the NiN-mode for conduction current density of 50 A/cm<sup>2</sup>. Increasing the pulse frequency up to MHz range, the optimum average forward voltage drop was significantly improved.

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